(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 630 044 A2**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: **94114930.4**

(51) Int. Cl.5: **H01L 21/90**

(22) Date of filing: **15.08.89**

This application was filed on 22 - 09 - 1994 as a divisional application to the application mentioned under INID code 60.

(30) Priority: **08.09.88 JP 223503/88**

(43) Date of publication of application:
21.12.94 Bulletin 94/51

(60) Publication number of the earlier application in accordance with Art.76 EPC: **0 358 350**

(84) Designated Contracting States:
DE FR GB

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(54) Forming a prescribed pattern on a semiconducor device layer.

(57) A method for forming a prescribed pattern on a layer of a semiconductor device, comprising the steps of:

preparing a substrate (40) having a first main surface;

forming a first layer (41) on the first main surface;

forming a second layer (42) on the first layer;

forming a third layer (43) on the second layer;

selectively removing the third layer to form a first patterned layer;

immersing the substrate having the first patterned layer into a predetermined solution to form a fourth layer (45) selectively over the portions of the second layer uncovered by the first patterned layer;

removing the first patterned layer; and

etching the second layer using the fourth layer (45) as a mask,

characterised in that the first layer (41) is an insulating layer, the second layer (42) is a metal layer, third layer (43) is a photoresist layer, and the fourth layer is a SiO_2 layer, whereby the remainder of the second layer (42) constitutes a metal interconnect layer for the semiconductor device.

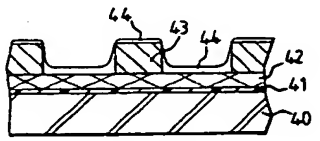

FIG.4A

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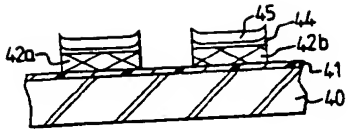

FIG.4D

This invention concerns a method for forming a prescribed pattern of, e.g., a wiring layer by etching, on a semiconductor device.

Conventionally, for etching a semiconductor substrate, a Reactive Ion Etching (**RIE**) is utilized using a photoresist pattern formed on the semiconductor substrate as a mask.

FIG.1 is a diagram for explaining a problem which is present in a conventional process for forming a pattern of submicron dimensions using a conventional exposure and development technique. Namely, in the case where the width between the adjacent pattern is relatively wide, e.g. 1.0 μm, a desired pattern may be obtained by the conventional technique. However, in the case where the width is 0.8 μm (e.g., between the photoresist pattern **12** and **13**), some undeveloped photoresist remains on the substrate **10**, since the bottom portion of the photoresist is not sufficiently exposed even if the upper portion is clearly patterned. Thus, it is difficult to use the photoresist pattern **12** and **13** as a mask in a subsequent etching process.

FIGS.2A and **2B** are diagrams for explaining a problem in a conventional process for forming a prescribed pattern of a high reflective metal layer **21** in a recessed portion **24** of a semiconductor substrate **20**. In the conventional process, a material of high reflectivity, such as a tungsten silicide 21, is formed. A photoresist layer 23 is then formed thereon (Fig. 2A). Next, an exposure and a development are carried out to form a photoresist pattern 23a and 23b. By this process, a desired pattern 23a and 23b of photoresist may be formed on a flat surface of the substrate 20. However, at the level difference portion 24, the reflected light from the angled surface 22 of the metal layer 21 exposes the photoresist 23 in the recess. Thus, the desired pattern illustrated by the dotted line 23c cannot be obtained, and a photoresist pattern 23d may result instead. Therefore, it is also difficult to use the pattern 23d as a mask to etch the metal layer 21 accurately.

It is known from U.S. Patent No. 4599137 to provide a method, as defined in the pre-characterizing portion of Claim 1, of forming a resist micropattern in a semiconductor device manufacturing process. Further, U.S. Patent No. 4624 749 discloses the use of a metal (gold) as an interconnect layer, formed by gold-electroplating selectively over a photoresist pattern which is complementary to the desired gold interconnect pattern.

An object of the present invention is to provide an improved method which results in a desired accurate photoresist pattern, even if the width between the adjacent portions of the pattern is of the submicron order.

To achieve the object, this invention provides a method as defined in Claim 1 and in Claim 2 for forming a prescribed pattern on a layer of a semiconductor device.

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention, and, together with the description, serve to explain the principles of the invention. Referring now to the drawings, like reference characters designate like or corresponding parts throughout the several views. Of the drawings:

FIG. 1 is a cross sectional view for explaining a problem in a conventional process.

FIGS. 2A and 2B are drawings for explaining another conventional process and the problem inherent therein.

FIGS. 3A to 3D are cross sectional views for explaining an embodiment of the present invention.

FIGS. 4A to 4D, FIGS. 5A to 5E, FIGS. 6A to 6D and FIGS 7A to 7D are cross sectional views of structures not made using the present invention but included for background information.

Referring now to the drawings, the present invention will be explained in detail.

FIGS. 3A to 3D are cross sectional views for explaining an embodiment of the present invention, which allows formation of a wiring pattern at a recessed portion of a semiconductor substrate.

At first, a semiconductor substrate **30** having a recessed portion or a dent **34** is prepared. Then, a tungsten silicide layer **31** to be patterned is formed on the substrate **31**. Next, a positive photoresist layer, e.g., an OFPR (manufactured by Tokyo Oka Co.), is formed over the entire surface, and a photoresist pattern **33a** and **33b** covering a wall **32** at the dent **34** is formed using a conventional exposure and development technique. (**FIG .3A**)

Next, the substrate **30** is immersed into a silicofluoride aqueous solution. In this step, a silicon oxide (SiO2) layer **35** of about 1000 Å is selectively formed at the area where the tungsten silicide (WSi) layer **31** is exposed, since the H2SiF6 and H2O react to precipitate SiO2. To selectively form the SiO2 layer, the surface of the photoresist layer **33a** and **33b** are subjected to, e.g., an oxygen plasma, to change the surface thereof from a hydrophilic condition (having, e.g., -OH radical as an end radical) to a hydrophobic condition (having, e.g., -O radical as an end radical), preferably. (**FIG.3B**) This process is referred to as a hydrophobic treatment hereafter.

Then, the photoresist pattern **33a** and **33b** are removed by, e.g., an ashing. (**FIG.3C**)

Next, an anisotropic etching, such as a **RIE**, is carried out to form a desired WSi wiring layer **31a**, **31b** and **31c** using the SiO2 layer **35** as a mask. (**FIG.3D**) Then, an etching for removing the SiO2 layer **35** follows thereafter. (not shown)

According to this process, the wall **32** at the

dent 34 is not exposed. Thus, the problem due to the light reflection from the surface 32 can be prevented. Furthermore, the etching selectively between the WSi and the Si02 is relatively high. Therefore, it is possible to obtain a desired pattern of WSi wiring 31a on the substrate 30, even if the substrate 30 includes a recessed portion, since the Si02 layer 35 having a relatively low etching rate is used as a mask to etch the WSi layer 31.

It is, of course, possible to use other materials for the wiring layer, as one of ordinary skill in this art will realise.

The following description is included as background, even though the examples do not embody the invention.

FIGS. 4A to 4D are cross sectional views. On a semiconductor substrate 40, a thermal oxide layer 41 is formed. On the oxide layer 41, an aluminium layer (A1) 42 of about 8000 A to be etched is formed by, e.g., sputtering. Then, a patterned photoresist pattern 43 of about 12,000 A is formed on the A1 layer 42 using a conventional exposure and development technique. Next, a glass layer 44 is formed by a Spin on Glass (SOG) method following a baking treatment. (FIG. 4A) Then, a conventional etching process is carried out to remove the relatively thin glass layer formed on the photoresist 43, and to leave a portion of the relatively thick glass layer 44 formed where the photoresist layer 43 is not formed. Next, a hydrophobic treatment is carried out.

Then, the substrate is immersed into a silicofluoride aqueous solution to form a Si02 pattern 45 of about 2000 A on the glass layer 44, selectively. (FIG 4B)

Next, the photoresist pattern 43 is removed by, e.g., a wet etching. (FIG. 4C)

Then, an anisotropic etching, e.g., a RIE, is carried out

to form a desired Al wiring layer **42a** and **42b** using the SiO2 pattern **45** as a mask. (**FIG.4D**) Then, an etching for removing the SiO2 layer **45** and the glass layer **44** is carried out (not shown).

In this process, the etching selectivity between the Al layer and the SiO2 layer is about 10, and is relatively large compared with that of between the Al layer and the photoresist layer, namely about 2. Thus, the selectivity of the etching can be improved. Furthermore, the remaining Al pattern **42a** and **42b** is determined by the SiO2 layer **45**. The area where the SiO2 layer is formed is determined by the remaining photoresist layer **43**. Thus, the narrower the photoresist pattern **43** becomes, the wider the Al pattern **42a** and **42b** becomes. It is easy to make the remaining photoresist pattern narrower by controlling the exposing condition, e.g. by an over exposure, since the photoresist is a positive photoresist. This means that the width between the adjacent patterns can be made narrower, and the resolution can be improved.

In this process, the glass layer **44** serves to protect the Al layer **42** from etching during the immersion of the substrate into the solution for precipitating the SiO2 layer **42**.

FIGS.5A to **5E** are drawings of a further example.

On a semiconductor substrate **50**, a thermal oxide layer **51** is formed. On the oxide layer **51**, a aluminium layer (Al) **52** of about 8,000 Å to be etched is formed by, e.g., a sputtering. Then, a glass layer **53** is formed by a Spin on Glass method following a baking treatment. Then, a patterned photoresist layer **54a**, **54b** and **54c** is formed using a conventional exposure and development technique. (**FIG.5A**)

After a hydrophobic treatment of the photoresist pattern 54, the substrate is immersed into a silicofluoride aqueous solution to form a SiO2 layer **55**. (**FIG.5B**)

Then, the resist layer **54** is removed. (**FIG.5C**)

Next, an etching, e.g., a wet etching, is carried out to etch the glass layer **53** using the SiO2 layer **55** as a mask. (**FIG.5D**)

Then, an anisotropic etching, e.g., a **RIE** etching, is carried out to ford a desired Al wiring layer 52a and 52b using the SiO2 layer **55** as a mask. (**FIG.5E**) Then, the glass layer **53** and the SiO2 layer **55** are removed (not shown). Using this process, a desired wiring pattern can be achieved, as in the example illustrated in **FIGS.4A** to **4D**.

FIGS.6A to **6D** are drawings for explaining a further example of forming a contact hole in a semiconductor device. On a semiconductor substrate **60**, an insulating layer **61** is formed. Then, a polysilicon layer **62** of about 300 Å is formed on the insulating layer by, e.g., a low pressure CVD method. Next, a patterned photoresist layer **63** is formed on the polysilicon layer **62** using a conventional exposure and development technique. (**FIG.6A**) Then, a hydrophobic treatment of the photoresist layer **63** is carried out.

Next, the substrate is immersed into a solution of palladium chloride (PbCl2) to form a palladium layer **64** of less than 100 Å using a non-electric plating method. Next, the substrate is immersed into a mixed solution of nickel sulfate (NiSO4) and hypophosphite to form a nickel layer **65** of about 1000 Å. (**FIG.6B**)

Next, the photoresist layer is removed by, e.g., an ashing treatment using an oxygen plasma. **FIG.6C**)

Then, an anisotropic etching, e.g., a **RIE**, is carried out to form a contact hole **66** using the nickel layer **65** as a mask. (**FIG.6D**)

Next, the nickel layer **65** and the palladium layer **64** are removed by a wet etching using a

mixed etchant of a hydrochloric acid, a nitric acid and an acetic acid. The polysilicon layer **62** may either be removed by a wet etching using an organic alkali solution, e.g., a choline or a dry etching using a fluorine as an active radical, or it may be oxidized and left as it is.

In this example, the size of the contact hole **66** is determined by the remaining photoresist pattern **63**. Thus, by narrowing the size of the photoresist layer **63** using, e.g., an over exposure, it is possible to form a resist pattern having a narrower width than the resolution limit. Thus, it is possible to form a narrower contact hole than when the conventional etching process is used. Furthermore, the etching rate of the nickel layer **65** is extremely smaller than that of the insulating layer **61**. Thus, a desired fine contact hole can be formed easily. The palladium layer **64** provides a good adhesion between the polysilicon layer **62** and the nickel layer **65**.

FIGS.7A to **7D** are drawings for explaining a further example of oxidizing a semiconductor substrate **70**. On a semiconductor substrate **70**, a thermal insulating layer **71** is formed. Then, a silicon nitride layer **72** is formed on the insulating layer **71**. Next, on the silicon nitride layer **72**, a patterned photoresist layer **73** is formed. (**FIG.7A**)

After a hydrophobic treatment of the photoresist layer **73**, the substrate is immersed into the same solution, in the same way, as the embodiment of **FIGS.3A** to **3D**, to form a SiO2 layer 74.

Next, the photoresist layer **73** is removed by, e.g., ashing using an oxygen plasma. (**FIG.7C**)

Then, the silicon nitride layer **72** is selectively etched by using the SiO2 layer **74** as a mask. An oxidizing treatment is then carried out to oxidize the substrate **70** to form a device separating oxide layer **75**, using the silicon nitride layer **72** selectively remaining under the SiO2 layer **74** as a mask layer. (**FIG.7D**) Next, an etching treatment, e.g., a Chemical pry Etching (**CDE**) is carried out to remove the SiO2 layer **74** and the silicon nitride layer **72**.

In the examples of Figures 3, 4, 5 and 7, a SiO2 layer formed by a precipitation is used as a mask layer. However, it is possible to use a nickel layer formed by a non-electric plating process, as used in Fig. 6, as a mask layer, and vice versa. Thus, in each example, either a SiO2 layer or a nickel layer may be used as the mask layer.

Furthermore, it is possible to etch the semiconductor substrate instead or the wiring layer and the insulating layer.

Moreover, it is possible to utilize the present invention to form a pattern on an optical disk for storing a information.

In the aforementioned examples, a photoresist layer is used for the pattern formation. However, any film layer can be used as long as the layer permits little or no precipitation of substances thereon during immersion.

The present invention has been described with respect to a specific embodiment. However, other embodiments should be apparent to those of ordinary skill in the art. Such embodiments are intended to be covered by the claims.

Claims

1. A method for forming a prescribed pattern on a layer of a semiconductor device, comprising the steps of:

   preparing a substrate (40) having a first main surface;

   forming a first layer (41) on the first main surface;

   forming a second layer (42) on the first layer;

   forming a third layer (43) on the second layer;

   selectively removing the third layer to form a first patterned layer;

   immersing the substrate having the first patterned layer into a predetermined solution to form a fourth layer (45) selectively over the portions of the second layer uncovered by the first patterned layer;

   removing the first patterned layer; and

   etching the second layer using the fourth layer (45) as a mask,

   characterised in that the first layer (41) is an insulating layer, the second layer (42) is a metal layer, third layer (43) is a photoresist layer, and the fourth layer is a $Si0_2$ layer, whereby the remainder of the second layer (42) constitutes a metal interconnect layer for the semiconductor device.

2. A method for forming a prescribed pattern on a layer of a semiconductor device, comprising the steps of:

   preparing a substrate (40) having a first main surface;

   forming a first layer (41) on the first main surface;

   forming a second layer (42) on the first layer;

   forming a third layer (43) on the second layer;

   selectively removing the third layer to form a first patterned layer, immersing the substrate having the first patterned layer into a predetermined solution to form a fourth layer (45) selectively over the portions of the second layer uncovered by the first patterned layer;

   removing the first patterned layer; and

   etching the second layer using the fourth

layer (45) as a mask;

characterised in that the first layer (41) is an insulating layer, the second layer (42) is a metal layer, third layer (43) is a photoresist layer, and the fourth layer is a metal layer, whereby the remainder of the second layer (42) constitutes a metal interconnect layer for the semiconductor device.

3. A method according to claim 1, further comprising the step of forming a glass layer (44) on the second layer (42) before the formation of the fourth layer (45).

4. A method according to claim 3, wherein the glass layer (44) is formed by a Spin on Glass method.

5. A method according to claim 1, further comprising the step of forming a sixth layer (53) as the upper layer of the second layer (52) before the formation of the third layer (54), so that the sixth layer is etched using the fourth layer (55) as a mask.

6. A method according to claim 2, wherein the fourth layer (65) is a nickel layer.

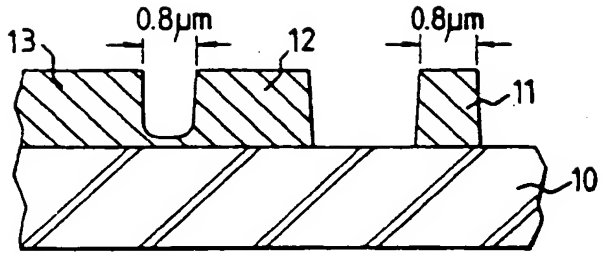

FIG.1
PRIOR ART

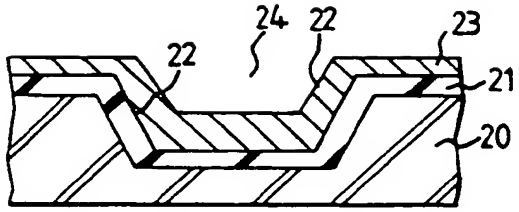

FIG.2A

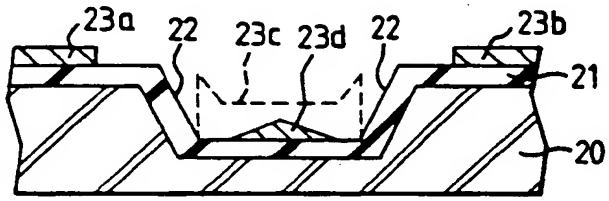

FIG.2B
PRIOR ART

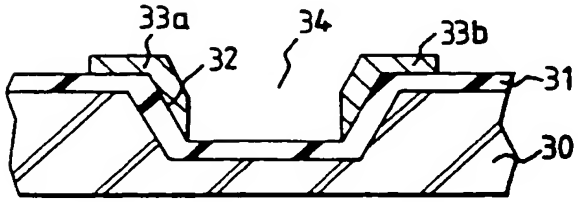

FIG.3A

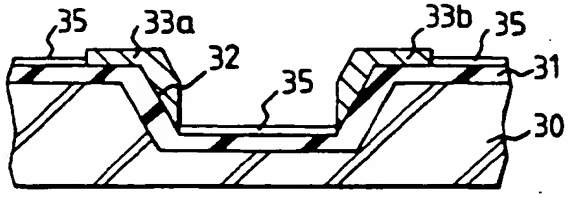

FIG.3B

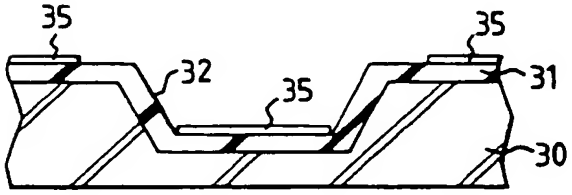

FIG.3C

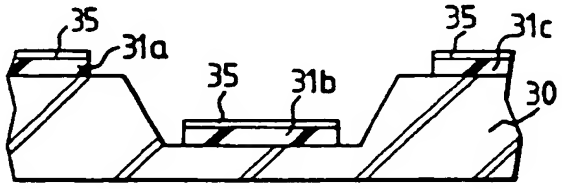

FIG.3D

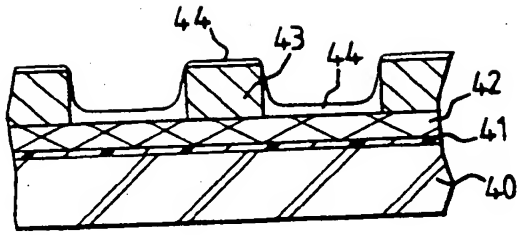

FIG.4A

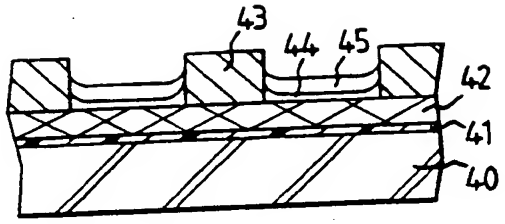

FIG.4B

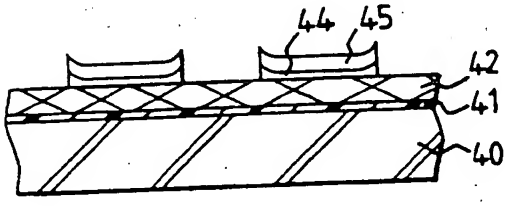

FIG.4C

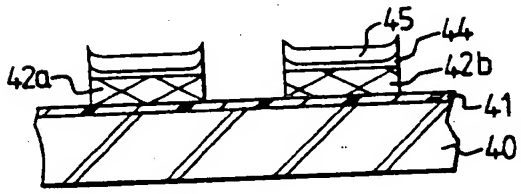

FIG.4D

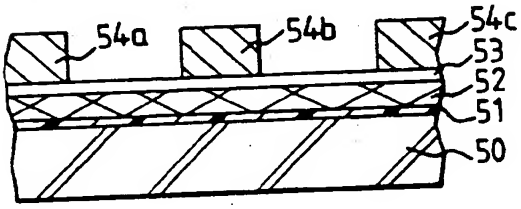

FIG.5A

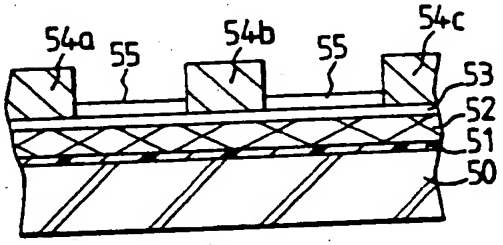

FIG.5B

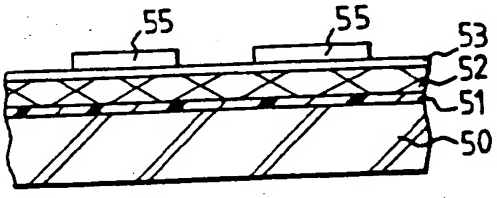

FIG.5C

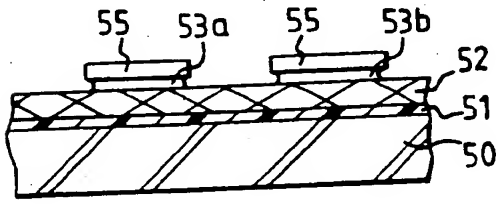

FIG.5D

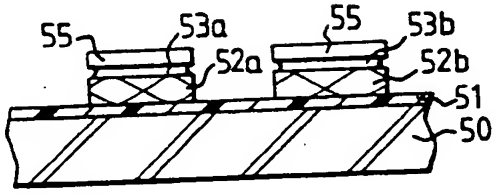

FIG.5E

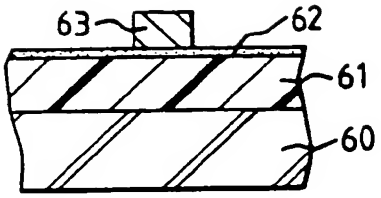

FIG.6A

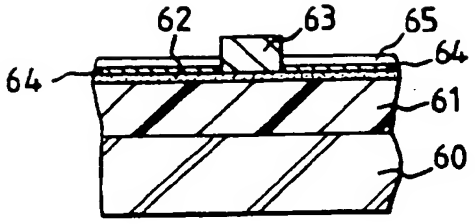

FIG.6B

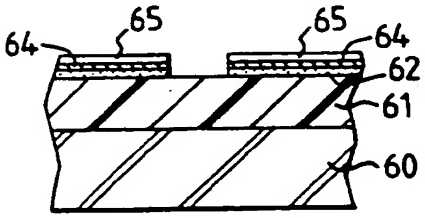

FIG.6C

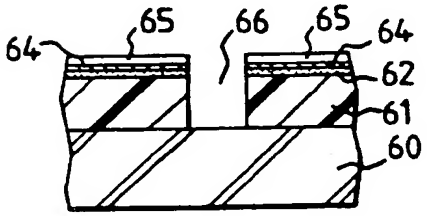

FIG.6D

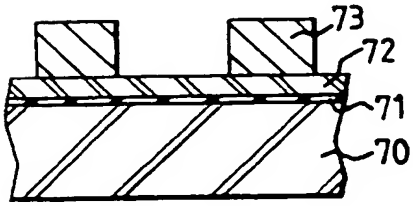

FIG.7A

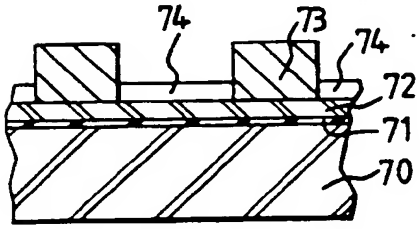

FIG.7B

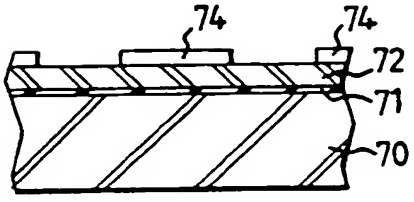

FIG.7C

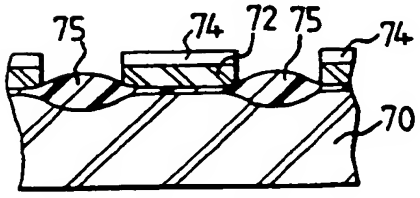

FIG.7D

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) Publication number: **0 630 044 A3**

(12) EUROPEAN PATENT APPLICATION

(21) Application number: 94114930.4

(51) Int. Cl.[6]: **H01L 21/90**, H01L 21/321

(22) Date of filing: **15.08.89**

(30) Priority: **08.09.88 JP 223503/88**

(43) Date of publication of application:
21.12.94 Bulletin 94/51

(60) Publication number of the earlier application in accordance with Art.76 EPC: **0 358 350**

(84) Designated Contracting States:
DE FR GB

(88) Date of deferred publication of the search report:
12.07.95 Bulletin 95/28

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(54) Forming a prescribed pattern on a semiconducor device layer.

(57) A method for forming a prescribed pattern on a layer of a semiconductor device, comprising the steps of:

preparing a substrate (40) having a first main surface;

forming a first layer (41) on the first main surface;

forming a second layer (42) on the first layer;

forming a third layer (43) on the second layer;

selectively removing the third layer to form a first patterned layer;

immersing the substrate having the first patterned layer into a predetermined solution to form a fourth layer (45) selectively over the portions of the second layer uncovered by the first patterned layer;

removing the first patterned layer; and

etching the second layer using the fourth layer (45) as a mask,

characterised in that the first layer (41) is an insulating layer, the second layer (42) is a metal layer, third layer (43) is a photoresist layer, and the fourth layer is a SiO_2 layer, whereby the remainder of the second layer (42) constitutes a metal interconnect layer for the semiconductor device.

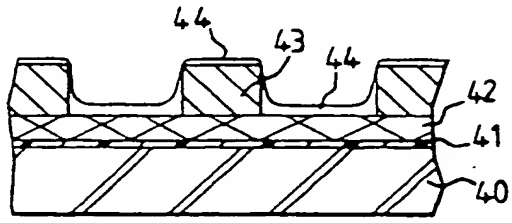

FIG.4A

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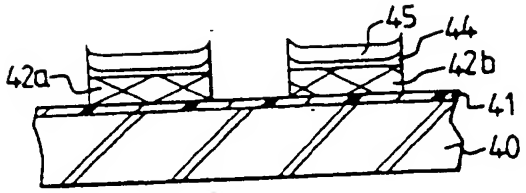

FIG.4D

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 94 11 4930

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.5)
X	FR-A-2 354 633 (IBM) * page 3, line 8 - page 4, line 37; figures 1-6 *	2,6	H01L21/90 H01L21/321
X,D	US-A-4 624 749 (HARRIS) * figures 1-6 *	2,6	
A,D	US-A-4 599 137 (NTT) * figure 1 *	1	
P,X	EP-A-0 304 077 (TOSHIBA) * abstract; figures *	1	
A	EP-A-0 178 619 (TOSHIBA) * abstract; figures 4,5 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.5)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 May 1995	Gori, P

CATEGORY OF CITED DOCUMENTS

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